**LAB EXPERIMENT 7**

**Aim:** To design test benches of SR Flip Flop,3:8 Decoder, Half Adder and Full Adder.

**Verilog Code of the Program**

1. **SR Flip Flop:**
2. **Verilog Code of the Program:**

module SR\_FlipFlop\_TestBench;  
// Inputs  
reg s;  
reg r;  
reg clk;  
// Outputs  
wire q;  
wire qbar;  
// Instantiate the Unit Under Test (UUT)  
SR\_FlipFlop\_BehavorialModelling uut (  
.s(s),  
.r(r),  
.clk(clk),  
.q(q),  
.qbar(qbar)  
);  
   initial begin  
clk = 0;  
forever #10 clk = ~clk;  
end  
initial begin  
 s= 0;  
 r= 0;  
 #5 s= 0;  
 r= 1;  
 #20 s= 1;  
 r= 0;  
 #20 s= 1;  
 r=1;  
 #20 $finish;  
end  
initial  
$monitor("s=%0d r=%0d q=%0d, qbar=%d, simtime=%g, clk=%b",s,r,q,qbar,$time,clk);  
endmodule

1. **Screenshot of the Program and Outputs:**

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1. **Half Adder**
2. **Verilog Code of Programming:**

module half\_tb;

// Inputs

reg inp1;

reg inp2;

// Outputs

wire outs;

wire outc;

// Instantiate the Unit Under Test (UUT)

DFMhalfadder uut (

.inp1(inp1),

.inp2(inp2),

.outs(outs),

.outc(outc)

);

initial begin

// Initialize Inputs

inp1 = 0;

inp2 = 0;

// Wait 100 ns for global reset to finish

#100

inp1 = 1;

inp2 = 0;

end

      endmodule

1. **Screenshot of the Program and Outputs:**

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Graphical user interface

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1. **Full Adder**
2. **Verilog Code of the Program :**

FULLADDERDFM18070123062 uut (

.x(x),

.y(y),

.cin(cin),

.s(s),

.c(c)

);

x = 0;

y = 0;

cin = 0;

#20 x = 0;

#15 y = 0;

#10 cin = 1;

#20 x = 0;

#15 y = 1;

#10 cin = 0;

#20 x = 0;

#15 y = 1;

#10 cin = 1;

#20 x = 1;

#15 y = 0;

# 10 cin = 0;

#20 x = 1;

#15 y = 0;

# 10 cin = 1;

#20 x = 1;

#15 y = 1;

# 10 cin = 0;

#20 x = 1;

#15 y = 1;

#10 cin = 1;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

end

endmodule

1. **Screenshot of the Program code and Output:**

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1. **3:8 Decoder**
2. **Verilog Code of the Program:**

module testbench\_decoder3to8;

// Inputs

reg s2;

reg s1;

reg s0;

// Outputs

wire d0;

wire d1;

wire d2;

wire d3;

wire d4;

wire d5;

wire d6;

wire d7;

// Instantiate the Unit Under Test (UUT)

decoder3to8\_062 uut (

.s2(s2),

.s1(s1),

.s0(s0),

.d0(d0),

.d1(d1),

.d2(d2),

.d3(d3),

.d4(d4),

.d5(d5),

.d6(d6),

.d7(d7)

);

initial begin

// Initialize Inputs

s2 = 0;

s1 = 0;

s0 = 0;

#10 s2=0;

#5 s1=0;

#10 s0=1;

#10 s2=0;

#5 s1=1;

#10 s0=0;

#10 s2=0;

#5 s1=1;

#10 s0=1;

#10 s2=1;

#5 s1=0;

#10 s0=0;

#10 s2=1;

#5 s1=1;

#10 s0=0;

#10 s2=1;

#5 s1=1;

#10 s0=1;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

end

endmodule

1. **Screenshot of the program code and Outputs:**

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Description automatically generated

**Conclusion**: From this experiment we learnt how to code testbenches of the verilog module we have created.